

What Is Claimed Is:

- Sub A1
1. A bus system for a unit, comprising:
 - a plurality of electrically independent bus segments; and
 - a plurality of nodes separating the bus segments and actively connecting and disconnecting at least two of the plurality of bus segments via at least one of i) a gate, ii) a switching element, iii) a driver, and iv) a register, each of the nodes including:
 - a respective routing table storing setup information for connections, and
 - a respective monitoring unit independently verifying whether a connection can be set up.
 2. The bus system according to claim 1, wherein the unit has a multi-dimensional cell architecture.
 - Sub C1
 3. The bus system according to claim 1, wherein the unit includes a plurality of CPUs in a multi-dimensional arrangement.
 4. The bus system according to claim 1, wherein the unit includes a plurality of arithmetic logic units in a multi-dimensional arrangement.
 - 12
 5. The bus system according to claim 2, wherein the unit having the multi-dimensional programmable cell architecture includes at least one of a field programmable gate array and a dynamically configurable gate array.
 - Sub A2
 6. The bus system according to claim 2, wherein the unit having the multi-dimensional programmable cell architecture includes a unit having a two-dimensional programmable cell architecture.
 7. The bus system according to claim 1, further

comprising:

a data transmitter setting up only a first connection to a first node of the plurality of nodes, the first node determining a second connection to a second node of the plurality of nodes via a first bus segment of the plurality of bus segments as a function of the respective routing table of the first node, the second node neighboring the first node,

wherein the first node establishes the second connection to the second node if the second node is not busy with another connection, and

wherein the first node performs at least one of an abortion and a termination of the second connection to the second node if the second node is busy with another connection.

56. The bus system according to claim 1, wherein the data transmitter provides a data packet to the first node, the first node sets up the first bus segment for transmitting the data packet, wherein the first node transmits the data packet to the second node via the first bus segment if the second node is not busy with another connection, the data packet being cleared in the first node, and the data packet being processed by the second node.

57. The bus system according to claim 1, wherein the first node determines the second connection to the second node as a function of at least one of a data address and a connection address by translating the at least one of the data address and the connection address to an address of the second node as a function of a lookup table.

58. The bus system according to claim 1, wherein the first node determines the second connection to the second node as a function of at least one of a data address and a connection address by performing at least one of a calculation of an address of the second node and a

A2
end

generation of the address of the second node via a lookup table.

8
11. The bus system according to claim 7, wherein the first node makes a second attempt to establish the second connection to the second node at a later predetermined time if a first attempt to establish the second connection was unsuccessful.

9
12. The bus system according to claim 7, wherein the first node establishes the second connection to the second node, the data transmitter transmitting a data packet to the second node via the first node, wherein the data transmitter exclusively controls the transmission of the data packet, and wherein the first node and the second node are passive during the transmission of the data packet.

10
13. The bus system according to claim 7, wherein the first node establishes the second connection to the second node, the data transmitter transmitting a data packet to the first node and the first node transmitting the data packet to the second node, the first node synchronizing the transmission of the data packet to the second node.

Sub 43
14. The bus system according to claim 1, wherein at least one of the plurality of nodes is a data transmitter and at least another of the plurality of nodes is a data receiver, the data transmitter transmitting a data packet to the data receiver,

wherein the data transmitter and the data receiver are not involved in the performance of the at least one of the connection and the disconnection of the at least two bus segments by each one of the plurality of nodes, and wherein the data transmitter and the data receiver do not actively intervene in an operation of the

143
end
plurality of nodes.

Sub
C2/
15. ~~The bus system according to claim 1, further comprising:~~

~~a program loading unit, and~~

~~wherein the program loading unit performs at least one of a configuration and a reconfiguration for each one of the plurality of nodes and the respective routing table of each one of the plurality of nodes.~~

14
16. The bus system according to claim ¹¹~~15~~, wherein a feedback signal from each one of the plurality of nodes is provided to the program loading unit via the respective routing table.

Sub
A4/
17. The bus system according to claim 1, wherein a first node of the plurality of nodes simultaneously broadcasts a data packet to several other nodes of the plurality of nodes, wherein the several other nodes returns a plurality of sync signals to the first node, the plurality of sync signals including an adjustable masking and an adjustable Boolean logic linkage.

18. A method for transmitting data in a module, the method comprising the step of:

transmitting the data with synchronization via a plurality of bus segments of a multi-dimensional bus system,

wherein the plurality of bus segments are connectable in a plurality of configurations.

19. The method according to claim 18, wherein the module has a multi-dimensional cell architecture.

20. The method according to claim 18, wherein the module includes a plurality of CPUs in a multi-dimensional arrangement.

21. The method according to claim 18, wherein the module includes a plurality of arithmetic logic units in a multi-dimensional arrangement.

Sub
P5

22. The method according to claim 19, wherein the module having the multi-dimensional programmable cell architecture includes at least one of a field programmable gate array and a dynamically configurable gate array.

23. The method according to claim 19, wherein the module having the multi-dimensional programmable cell architecture includes a module having a two-dimensional programmable cell architecture.

Sub
C3

24. The method according to claim 18, wherein the plurality of bus segments are permanently connected to a continuous bus system without delays.

25. The method according to claim 18, wherein the plurality of bus segments are switched by a plurality of registers, each one of the plurality of registers having a time delay and an arbitration.

Sub
C4

27. The method according to claim 18, wherein the plurality of bus segments are at least one of permanently connected to a continuous bus system without delays and switched by a plurality of registers, each one of the plurality of registers having a time delay and an arbitration.

17

28. The method according to claim 18, the method further comprising the step of:

controlling a setup of the plurality of bus segments via a plurality of lookup tables, the plurality of lookup tables storing connection data,
wherein a first lookup table of the plurality

of lookup tables is referenced for an entry of a following second lookup table of the plurality of lookup tables.

Sub C5
29. ~~The method according to claim 18, the method further comprising the steps of:~~

~~entering at least one of a unique determinable relative address and a unique absolute address of a target; and~~

~~setting up the plurality of bus segments as a function of the unique determinable relative address and the unique absolute address.~~

29
30. The method according to claim ²³~~29~~, the method further comprising the steps of:

setting up the plurality of bus segments in a first direction;

changing the first direction only if an axis of the target is reached.

30
31. The method according to claim ²³~~29~~, the method further comprising the steps of:

setting up the plurality of bus segments in a first direction;

changing the first direction if a blockage is encountered.

31
32. The method according to claim ²³~~29~~, the method further comprising the step of:

setting up the plurality of bus segments in a first direction,

wherein none of the plurality of bus segments are set up that are located in a second direction, the second direction being opposite to the first direction, and wherein none of the plurality of bus segments are set up beyond an axis of the target.

32
33. The method according to claim 23, the method further comprising the step of:

setting up the plurality of bus segments in a first direction,

wherein a first bus segment of the plurality of bus segments is set up that is located in a second direction if the first bus segment is within a first fixed predetermined limit, the second direction being opposite to the first direction, and wherein a second bus segment of the plurality of bus segments is set up that is beyond an axis of the target if the second bus segment is within a second fixed predetermined limit.

Sub C6
34. The method according to claim 18, the method further comprising the step of:

setting up the plurality of bus segments as a function of at least one of a plurality of lookup tables and an at least one of a unique determinable relative address and a unique absolute address of a target.

35. The method according to claim 18, the method further comprising the step of:

setting up the plurality of bus segments via a plurality of requests to a plurality of nodes,

wherein a set of requests to a single node of the plurality of nodes are arbitrated if the set of requests includes more than one request.

36. The method according to claim 18, the method further comprising the step of:

setting up the plurality of bus segments via a plurality of requests to a plurality of nodes,

wherein a set of requests to a single node of the plurality of nodes are simultaneously processed by the single node.

37. The method according to claim 18, the method further

comprising the steps of:

providing data from a first node of a plurality of nodes to a second node of a plurality of nodes via a first bus segment of the plurality of bus segments; and providing a first acknowledgment from the ~~second node.~~

~~33~~²⁷. The method according to claim ~~37~~²⁷, the method further comprising the step of:

providing the data to at least a third node of the plurality of nodes;

providing a second acknowledgment from the third node; and

linking the first acknowledgment and the second acknowledgment with an at least one Boolean operator in a predetermined manner.

~~34~~²⁷. The method according to claim ~~37~~²⁷, the method further comprising the step of:

providing the data to at least a third node of the plurality of nodes;

providing a second acknowledgment from the third node; and

masking out one of the first acknowledgment and the second acknowledgment.

~~35~~²⁷. The method according to claim ~~37~~²⁷ the method further comprising the step of:

providing the data to at least a third node of the plurality of nodes;

providing a second acknowledgment from the third node; and

determining a resulting acknowledgment signal by performing at least one of a linking the first acknowledgment and the second acknowledgment with an at least one Boolean operator in a predetermined manner and a masking out one of the first acknowledgment and the

second acknowledgment.

Sub C7 41. The method according to claim 18, the method further comprising the steps of:

establishing a connection via at least one bus segment of the plurality of bus segments and at least one node of a plurality of nodes;

disconnecting the connection as a function of an interrupt signal; and

providing the interrupt signal to the at least one node

36 42. The method according to claim 41, the method further comprising the step of:

generating the interrupt signal when a predefined condition is satisfied.

Sub A6 43. The method according to claim 42, wherein the predefined condition is the at least one node exceeding a predetermined time limit.

44. The method according to claim 42, wherein the predefined condition is a predetermined time period in which no data is transmitted.

45. The method according to claim 42, wherein the predefined condition is a predetermined time period in which data is transmitted.

46. The method according to claim 42, wherein the predefined condition is a predetermined amount of data having been transmitted.

47. The method according to claim 42, wherein the predefined condition is at least one of the at least one node exceeding a predetermined time limit, a predetermined time period in which no data is

Ab
end

transmitted, a predetermined time period in which data is
transmitted, a predetermined amount of data having been
transmitted and a non-occurring condition.

09145139 082898
0602280 "GETST60